M5M5256CFP,VP,RV-12VLL,-15VLL, -12VXL,-15VXL

262144-BIT(32768-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

This M5M5256CFP, VP, RV is a 262144-bit CMOS static RAMs organized as 32768-words by 8-bits which is fabricated using high-performance 3 polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high-density and low-power static RAM. They are low stand-by current and low voltage operation (3V) and ideal for the battery operation application.

Especially the M5M5256CVP, RV are packaged in a 28-pin thin small outline package. Two types of devices are available, M5M5256CVP (normal lead bend type package) and M5M5256CRV (reverse lead bend type package). Using both type of devices, it becomes very easy to design a printed circuit board.

FEATURES

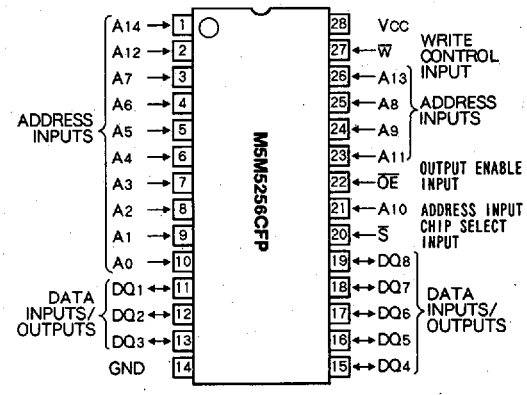
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5256CFP, VP, RV-12VLL M5M5256CFP, VP, RV-15VLL	120ns 150ns	50mA (Vcc=5.5V)	11 μA (Vcc = 3.3V)
M5M5256CFP, VP, RV-12VXL M5M5256CFP, VP, RV-15VXL	120ns 150ns	20mA (Vcc=3.3V)	2.2 μA (Vcc = 3.3V) 0.05 μA (Vcc = 3V, typ)

- Single +2.7~5.5V power supply
- No clocks, no refresh
- Data-hold on +2V power supply
- Directly TTL compatible : All inputs and outputs
- Three-state outputs : OR-tie capability
- Simple memory expansion by $\overline{S}$
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Low stand-by current ····· 0.05 μA (typ)
- Package
  - M5M5256CFP ····· 28 pin 450 mil SOP
  - M5M5256CVP, RV ····· 28pin 8 × 13.4mm² TSOP

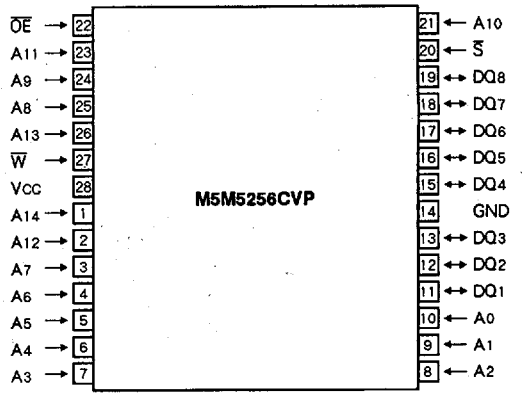
APPLICATION

Small capacity memory units

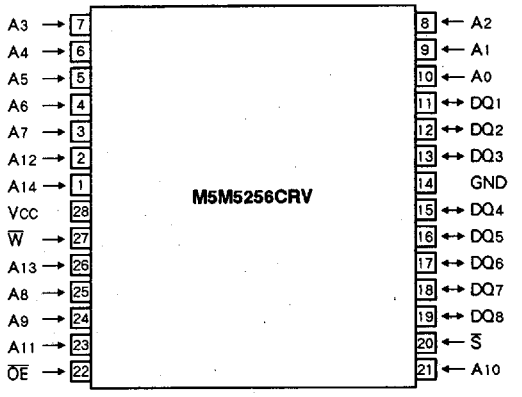
PIN CONFIGURATION (TOP VIEW)



Outline 28P2W-C



Outline 28P2C-A



Outline 28P2C-B

FUNCTION

The operation mode of the M5M5256CFP, VP, RV is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summariezed in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set-up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

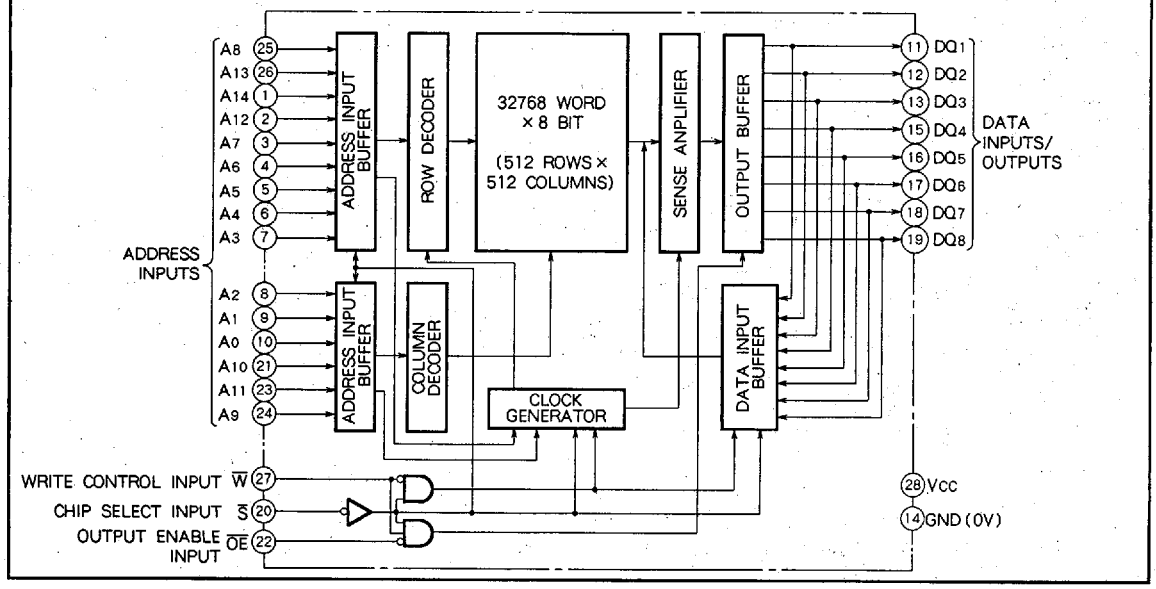
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state.

When setting $\overline{S}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	D_{in}	Active
L	H	L	Read	D_{out}	Active
L	H	H		High-impedance	Active

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3~7	V
V_I	Input voltage	With respect to GND	−0.3*~V_{CC}+0.3	V
V_O	Output voltage	With respect to GND	0~V_{CC}	V
P_d	Power dissipation	Ta = 25℃	700	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		−65~150	℃

* −3.0V in case of AC (Pulse width ≧ 30ns)

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 2.7~5.5V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits 1 (V_{CC} = 5V ± 10%) Min	Typ	Max	Limits 2 (V_{CC} = 3V ± 10%) Min	Typ	Max	Unit
V_{IH}	High-level input voltage			2.2		V_{CC}+0.3	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			−0.3*		0.8	−0.3*		0.6	V
V_{OH1}	High-level output voltage 1	I_{OH} = −1mA (V_{CC} = 5V ± 10%) I_{OH} = −0.5mA (V_{CC} = 3V ± 10%)		2.4			2.4			V
V_{OH2}	High-level output voltage 2	I_{OH} = −0.1mA (V_{CC} = 5V ± 10%) I_{OH} = −0.05mA (V_{CC} = 3V ± 10%)		V_{CC}−0.5			V_{CC}−0.5			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA (V_{CC} = 5V ± 10%) I_{OL} = 1mA (V_{CC} = 3V ± 10%)				0.4			0.4	V
I_I	Input leakage current	V_I = 0~V_{CC}				±1			±1	μA
I_O	Output leakage current	$\overline{S}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0~V_{CC}				±1			±1	μA
I_{CC1}	Active supply current (AC, MOS level)	$\overline{S}$ ≦ 0.2V Other inputs ≦ 0.2V or ≧ V_{CC} − 0.2V Output open	Min. cycle		30	45		10	20	mA
			1MHz		4	8		1.5	3	
I_{CC2}	Active supply current (AC, TTL level)	$\overline{S}$ = V_{IL}, Other inputs = V_{IL} or V_{IH} Output open	Min. cycle		35	50		10	20	mA
			1MHz		5	10		1.5	3	
I_{CC3}	Stand-by supply current	$\overline{S}$ ≧ V_{CC} − 0.2V, Other inputs = 0~V_{CC}	-VLL			20			11	μA
			-VXL		0.1	5		0.05	2.2	
I_{CC4}	Stand-by supply current	$\overline{S}$ = V_{IH}, Other inputs = 0~V_{CC}				3			0.3	mA

* −3.0V in case of AC (Pulse width ≦ 30ns)

CAPACITANCE (Ta = 0~70℃, V_{CC} = 2.7~5.5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Typ	Max	Unit
C_I	Input capacitance	V_I = GND, V_I = 25mV_{rms}, f = 1MHz			6	pF
C_O	Output capacitance	V_O = GND, V_O = 25mV_{rms}, f = 1MHz			8	pF

Note 1. Direction for current flowing into IC is indicated as positive. (no mark)
2. Typical value is V_{CC} = 5V or 3V, Ta = 25℃.
3. C_I, C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 2.7~5.5V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level ·····V_{IH} = 2.4V, V_{IL} = 0.6V (Vcc = 5V ± 10%)
V_{IH} = 2.2V, V_{IL} = 0.4V (Vcc = 3V ± 10%)
Input rise and fall time ·····5ns
Reference level ·····V_{OH} = V_{OL} = 1.5V
Transition is measured ± 500mV from steady state voltage.(for t_{en}, t_{dis})
Output loads ·····Fig.1, C_L = 100pF (FP, VP, RV-15VLL, -15VXL)
C_L = 50pF (FP, VP, RV-12VLL, -12VXL)
C_L = 5pF (for t_{en}, t_{dis})

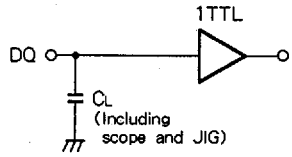


Fig.1 Output load

(2) READ CYCLE

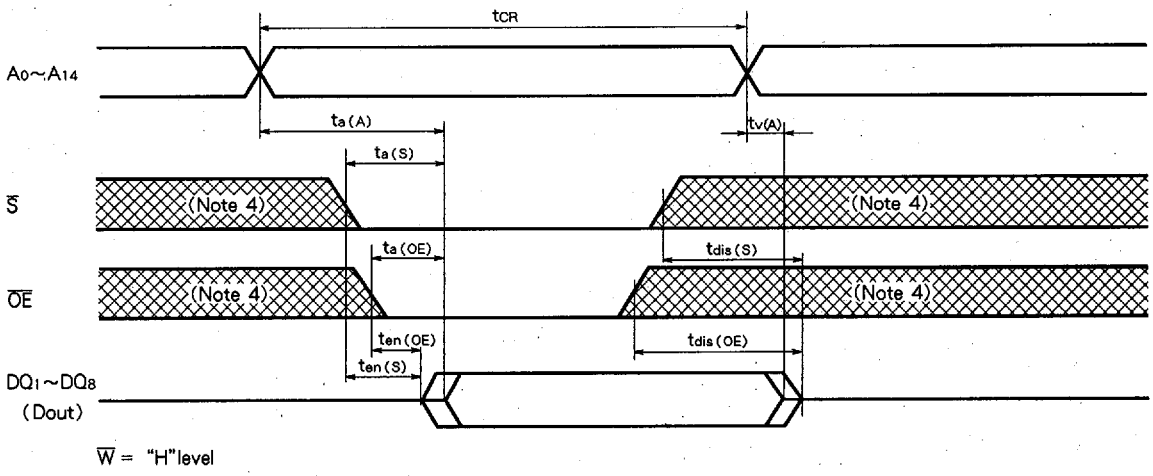
Symbol	Parameter	Limits						Unit
		M5M5256C-12VLL M5M5256C-12VXL			M5M5256C-15VLL M5M5256C-15VXL			
		Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	120			150			ns
$t_{a(A)}$	Address access time			120			150	ns
$t_{a(S)}$	Chip select access time			120			150	ns
$t_{a(OE)}$	Output enable access time			60			75	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high			35			40	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			35			40	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	10			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	10			10			ns
$t_{v(A)}$	Data valid time after address	10			10			ns

(3) WRITE CYCLE

Symbol	Parameter	Limits						Unit
		M5M5256C-12VLL M5M5256C-12VXL			M5M5256C-15VLL M5M5256C-15VXL			
		Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	120			150			ns
$t_{w(W)}$	Write pulse width	80			90			ns
$t_{su(A)}$	Address set up time	0			0			ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$ high	90			100			ns
$t_{su(S)}$	Chip select set up time	90			100			ns
$t_{su(D)}$	Data set up time	45			50			ns
$t_{h(D)}$	Data hold time	0			0			ns
$t_{rec(W)}$	Write recovery time	0			0			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low			35			40	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			35			40	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	10			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	10			10			ns

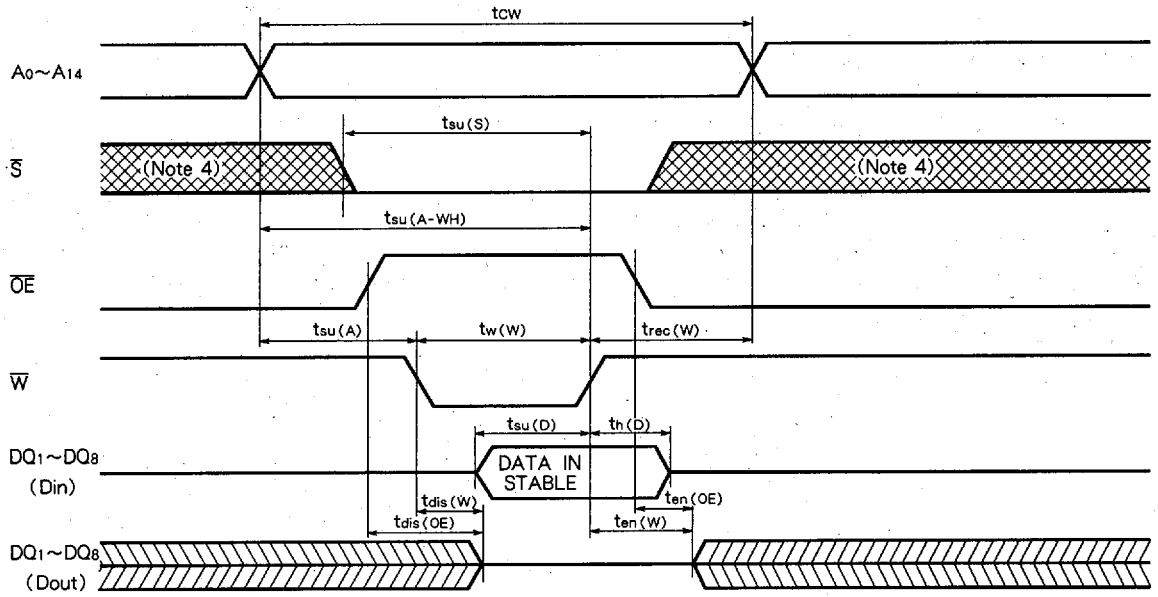
(4) TIMING DIAGRAMS

Read cycle

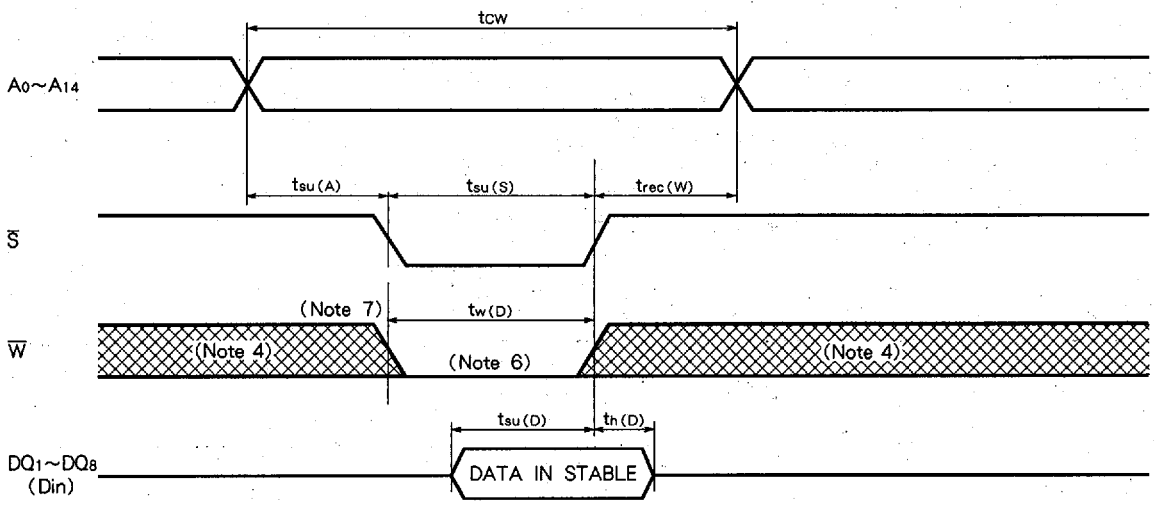


W = "H"level

Write cycle (W control mode)



Write cycle ($\overline{S}$ control mode)



Note 4. Hatching indicates the state is don't care.
5. Writing is executed in overlap of $\overline{S}$ and $\overline{W}$ low.
6. If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the high-impedance state.
7. Don't apply inverted phase signal externally when DQ pin is in output mode.
8. ten, tdis are periodically sampled and are not 100% tested.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S})}$	Chip select input $\overline{S}$	2.2V ≦ $V_{CC(PD)}$		2.2			V
		2V ≦ $V_{CC(PD)}$ ≦ 2.2V			$V_{CC(PD)}$		
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3V, Other inputs = 3V	-VLL			10*	μA
			-VXL		0.05	2**	

* Ta = 25℃, $I_{CC(PD)}$ = 1 μA
** Ta = 25℃, $I_{CC(PD)}$ = 0.2 μA

(2) TIMING REQUIREMENTS (T_a = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

(3) POWER DOWN CHARACTERISTICS
$\overline{S}$ control mode